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Design of 64-Bit Multiplier Based on Vedic Mathematics using VHDL

Miss. Pratiksha Awate[1], Prof. P. R. Indurkar[2]

Student M.Tech (VLSI), Department of E&T, BDCOE, Sewagram, Maharashtra, India[1]

Associate Professor, Department of E&T, BDCOE, Sewagram, Maharashtra, India[2]

Abstract: The need of high speed multiplier is increasing day by day on account of recent computer applications. As the multiplication takes considerably more amount of time for its calculation, the computation time must be reduced to get speedy results. To obtain the speedy results, either computation time must be reduced or the pace of the coprocessor must be improved. In this paper we have proposed a high speed 64-bit multiplier making use of Urdhava Tiryakbhyam Sutra of Vedic mathematics. Multiplier is one of the key hardware blocks in most Digital Signal Processing (DSP) systems. Furthermore, design of MAC unit which consists of Multiplier unit, Adder and Accumulator will be implemented. Design, synthesis and simulation of 64-bit MAC unit will be done using XILINX ISE 14.5. Coding of the proposed design will be done in VHDL (Very high Speed Integrated Circuit Hardware Description Language). Combinational path delay obtained for 64-bit Vedic multiplier is 7.970nsec with frequency of 125.467MHz.

Keywords: Urdhava Tiryakbhyam, Vedic Multiplier, XILINX ISE, VHDL.

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate (MAC) and inner product are among some of the frequently used computation Intensive Arithmetic Functions (CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filtering and in microprocessors in its arithmetic and logic unit. Multiplication can be implemented using several algorithms such as: array, Booth, modified Booth algorithms.Vedic Mathematics is a name which is heard many times with reference to the techniques for solving mathematics problem mentally. One of the main purposes of Vedic mathematics is to transform the tedious calculations into simpler, orally manageable operation without much help of pen and paper. Any ordinary human can perform mental operations for very small magnitude of numbers and hence Vedic mathematics provides techniques to solve operations with large magnitude of numbers easily. Vedic mathematics provides more than one method for multiplication operations. For each operation there is at least one generic method provided along with some methods which are directed towards specific cases simplifying the calculations further.

Vedic mathematics provides algorithms to simplify the mathematics and hence is perfect solution for the problem stated. After a thorough and comparative study we have found that Vedic multiplier designed by is better than other available multipliers. A MAC unit consists of a multiplier, adder and an accumulator containing the sum of the previous successive products. The MAC Unit obtain inputs from the memory location such as RAM and given to the Multiplier.MAC Unit is used in DSP Applications that uses discrete cosine transform (DCT) or Discrete Wavelet Transforms (DWT). Where, Multiplication is accomplished by repetitive application of addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire Calculation. The functionality of the MAC unit enables high-speed filtering and other processing which are typical for DSP applications. Particularly, in applications like optical Communication Systems which is based on DSP, require extremely fast processing of huge amount of digital data [2].

II. VEDIC MATHEMATICS

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means “Vertically and crosswise”. It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhava Triyakbhyam explained in fig 2.1. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in

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increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers.

Implementation Of 16x16 Bits Vedic Multiplier

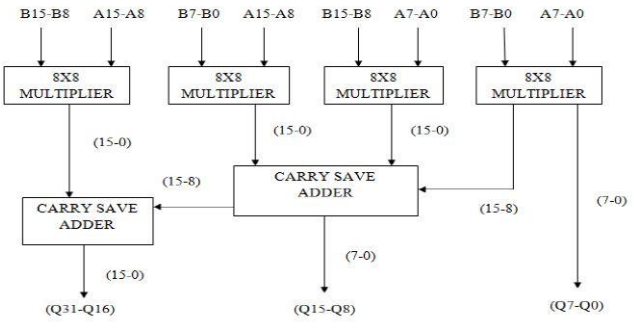

Figure 1: Implementation of 16x16 Bits Vedic Multiplier

The 16X16 bit multiplier structured using 8X8 bits blocks as shown in Figure 1. In this Figure the 16 bit multiplicand A can be decomposed into pair of 8 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The outputs of 8X8 bit multipliers are added accordingly to obtain the 32 bits final product. Thus, in the final stage two adders are also required.

Implementation Of 32x32 Bits Vedic Multiplier

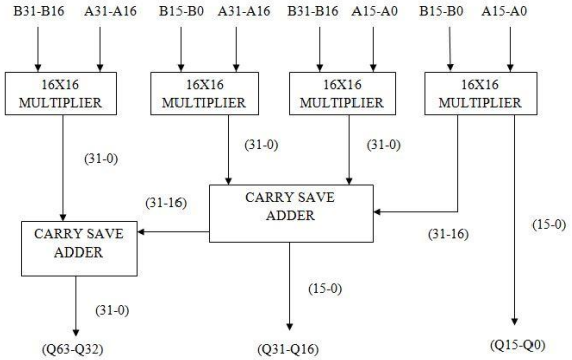

Figure 2: Implementation of 32x32 Bits Vedic Multiplier

The 32 bits multiplicand A is decomposed into pair of 16 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The outputs of 16X16 bit multipliers are added accordingly to obtain the 64 bits final product. Thus, in the final stage two adders are also required.

Implementation Of 64x64 Bits Vedic Multiplier

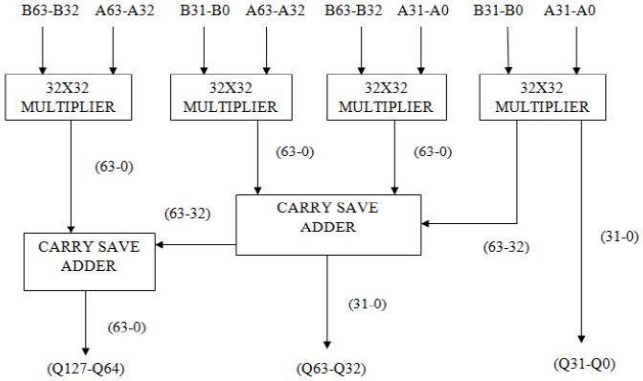

Figure 3: Implementation of 64x64 Bits Vedic Multiplier

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The 64 bits multiplicand A is decomposed into pair of 32 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The outputs of 32X32 bit multipliers are added accordingly to obtain the 128 bits final product. Thus, in the final stage two adders are also required.

III. PROPOSED DESIGN

The Proposed work is to design of High Speed Efficient 64-Bit Multiplier-And-Accumulator (MAC) based on Vedic Mathematics Using VHDL. High Speed Efficient 64-Bit Multiplier-And-Accumulator (MAC) can be composed with Vedic Multiplier, CSA adder, and Accumulator. Following figure shows a proposed block diagram of High Speed Efficient 64-Bit Multiplier-And-Accumulator (MAC) based on Vedic Mathematics Using VHDL.

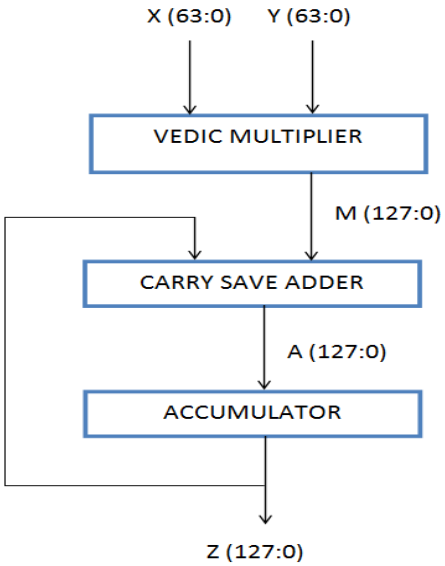

Figure 4: Proposed Diagram of 64-Bit MAC

The proposed work is likely to achieve the Vedic Multiplier, CSA adder, and Accumulator & Multiplier-And-Accumulator (MAC) based on Vedic Mathematics Using VHDL. Hence, 64-Bit Multiplier-And-Accumulator (MAC) based on Vedic Mathematics Using VHDL with high speed will be probable outcome of this research work.

IV. EXPERIMENTAL RESULTS

RTL View

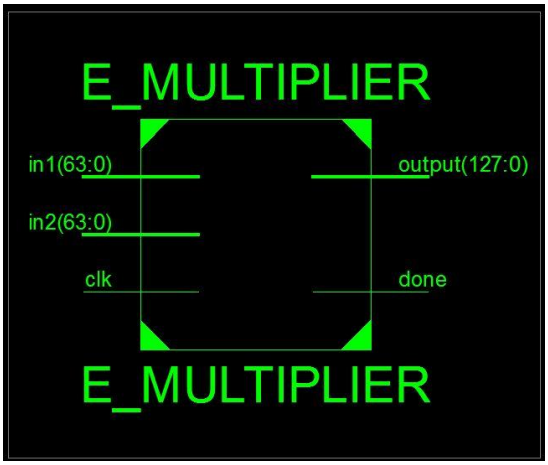

Figure 5: RTL View of 64-Bit Vedic Multiplier

Figure 5 shows RTL (Register Transfer Logic) view of 64-bit Vedic Multiplier with inputs in1, in2, clk and outputs as output, done.

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Simulation Result

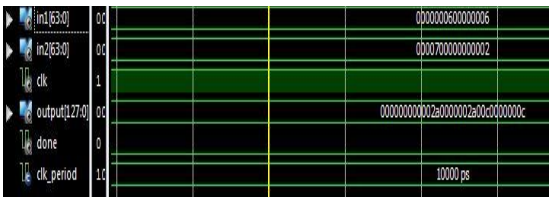

Figure 6: RTL View of 64-Bit Vedic Multiplier

Figure 6 shows Simulation Result of 64-bit Vedic Multiplier with inputs in1, in2, clk and outputs as output, done.

Comparison Table

Parameters	Delay (nsec)	No. of 4 input LUTs	No. of occupied slices
Proposed Multiplier	7.970	379	390
Reference [11]	29.967	2289	1817

V. CONCLUSION

In this paper we have discussed in detail about 64-bit multiplier based on Vedic Mathematics using VHDL. Design, synthesis and simulation of 64-bit Vedic Multiplier have been done using XILINX ISE 14.5. Coding of the proposed design has been done in VHDL. Combinational path delay obtained for 64-bit Vedic multiplier is 7.970nsec with frequency of 125.467MHz. Future work is likely to achieve the design, synthesis and simulation of CSA adder, Accumulator and finally the Multiplier-And-Accumulator (MAC) unit based on Vedic Mathematics Using VHDL. Therefore, 64-Bit Multiplier-And-Accumulator (MAC) based on Vedic Mathematics Using VHDL is the aim of this research work.

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